


In re patent application of: Chuan Hu and Daoqiang Lu
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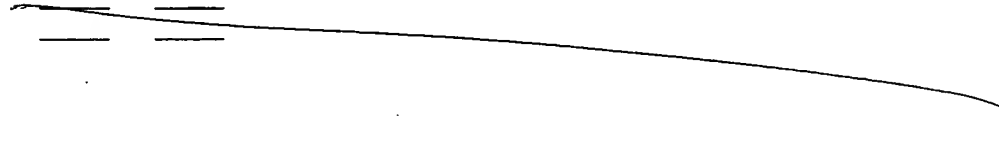
U.S. PATENT DOCUMENTS

Exam Init	Ref	Document Number	Issue Date	Name	Class	Sub Class
<u>DLG</u>	_____	6,471,115 B1	10/29/2002	Ijuin et al.		
<u>DLG</u>	_____	6,495,397 B2	12/17/2002	Kubota et al.		



FOREIGN PATENT DOCUMENTS

Exam Init	Ref	Document Number	Publication Date	Country	Name
_____	_____	_____	_____	_____	_____
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OTHER DOCUMENTS

Exam Init	Ref	Author, Title, Date, Pertinent Pages, Etc.)
<u>DLG</u>		Klink et al., "Innovative Packaging Concepts for Ultra Thin Integrated Circuits," <i>IEEE 2001 Electronic Components and Technology Conference</i> , 5 pages (2001).
<u>DLG</u>		Dodd et al., "Impact of Substrate Thickness on Single-Event Effects in Integrated Circuits," <i>IEEE Transactions on Nuclear Science</i> , Vol. 48, No. 6, p. 1865-1871 (December 2001).
<u>DLG</u>		Sunohara et al., "Development of Wafer Thinning and Double-Sided Bumping Technologies for the Three-Dimensional Stacked LSI," <i>IEEE 2002 Electronic Components and Technology Conference</i> , p. 238-245 (2002). http://www.webelements.com/webelements/elements/text/Au/enth.html .
<u>DLG</u>		Mark Winter, <i>The University of Sheffield</i> , 4 pages (3/6/2003). "Some Practical Suggestions for Solder Preform Design," <i>Indium Corporation of America</i> , 1 page (prior to 5/12/03). "Mechanical Enabling for the Intel® Pentium® 4 Processor in the 478-Pin Package," <i>Intel Corporation</i> (October 2001).

Examiner: Donald K. Jones

Date Considered: 1/22/05